UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/560,920	04/10/2007	Seong Ik. Jeong	GUA-0014-SE	2475

82727 7590 09/29/2010

Jae Y. Park
Kile, Park, Goekjian, Reed & McManus, PLLC
1200 New Hampshire Ave. NW, Suite 570
Washington, DC 20036

EXAMINER	
CHOW, YUK	

ART UNIT	PAPER NUMBER
2629	

MAIL DATE	DELIVERY MODE
09/29/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/560,920	JEONG, SEONG IK.	
	Examiner	Art Unit	
	YUK CHOW	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 December 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/14/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-4, 7-11, 14-16, 21-24, 29-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Kubota et al. (US 6,437,768).

As to **claim 1**, Kubota discloses a memory device for driving a display panel comprising:

arrays of memory cells (Fig. 1, latch circuits) storing binary information;

pairs of bit line-bit bar line connected to the memory cells (Fig. 3, pairs CKIi and CKIi bar connected to LATij and LATkj+1);

first transfer gates (Fig. 3(in)) connected to one end of the bit line-bit bar line pairs and switched to access the memory cells;

second transfer gates (Fig. 3(out)) connected to the other end of bit line-bit bar line pairs and switched to read out the binary information stored in the memory cells (see Col. 8 lines 28-39); and

data buffers (Fig. 1, buffers) to store the read-out binary information,

wherein signals switching the second transfer gates are derived from a single enable signal (see Fig. 9, switching the second transfer gates ($OUT1_1$ and OUT_2 are derived from a single enable signal ST) and divided into several groups, and the signal for each group has a different time delay (see Fig. 6, enable signal ST divided into groups L1-Ln).

As to **claim 2**, Kubota discloses a memory device for driving a display panel comprising:

a memory cell array (Fig. 1, latch circuits) storing binary information;

pairs of bit line-bit bar line connected to the memory cells (Fig. 3, pairs CKIi and CKIi bar connected to LATij and LATkj+1);

first transfer gates (Fig. 3(in)) connected to one end of the bit line-bit bar line pairs and switched to access the memory cells (see Col. 8 lines 28-39);

second transfer gates (Fig. 3(out)) connected to the other end of bit line-bit bar line pairs and switched to read out the binary information stored in the memory cells; and

data buffers (Fig. 1, buffers) to store the read-out binary information,

wherein signals enabling the data buffers are derived from a single enable signal (Fig. 1, Analog switch enables the data buffers, and are derived from a single enable signal ST) and divided into several groups, and the signal for each group has a different time delay (see Fig. 6, enable signal ST divided into groups L1-Ln).

As to **claim 3**, Kubota discloses a memory device for driving a display panel comprising:

a memory cell array (Fig. 1, latch circuits) storing binary information;

pairs of bit line-bit bar line connected to the memory cells (Fig. 3, pairs CKIi and CKIi bar connected to LATij and LATkj+1);

first transfer gates (Fig. 3(in)) connected to one end of the bit line-bit bar line pairs and switched to access the memory cells;

second transfer gates (Fig. 3(out)) connected to the other end of bit line-bit bar line pairs and switched to read out the binary information stored in the memory cells (see Col. 8 lines 28-39); and

data buffers (Fig. 1, buffers) to store the read-out binary information,

wherein signals enabling the data buffers (Fig. 1, Analog switch enables the data buffers) and signals switching the second transfer gates (see Fig. 9, switching the second transfer gates ($OUT1_1$ and OUT_2 are derived from a single enable signal ST) are

derived from a single enable signal and divided into several groups, and the signal for each group has a different time delay (see Fig. 6, enable signal ST divided into groups L1-Ln).

As to **claim 4**, Kubota discloses the memory device of claim 1, wherein the different time delay is performed by a circuit including a logic circuit having an inversing function (see Fig. 3(inverters)).

As to **claim 7**, Kubota discloses the memory device of claim 1, wherein the time delay is a signal generated by a plurality of delay portions which are connected in series (see Fig. 1, latch circuits are connected in series).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 5, 6, 12, 13, 17-20 and 25-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kubota et al. (US 6,437,768).

As to **claim 5**, Kubota discloses the memory device of claim 1.

However, Kubota does not teach the different time delay is performed by a capacitor, a resistor, or a combination of the capacitor and the resistor.

A capacitor or resistor are known components for constructing a time delay circuit, for instant, an RC oscillating circuit can performed time delay.

Therefore It would have been obvious to one ordinary skill in the art at the time of invention was made to us a capacitor, a resistor, or a combination of both to design a time delay circuit.

As to **claim 6**, Kubota discloses the memory device of claim 1.

However, Kubota does not teach the first transfer gates are switched by the column address as being grouped by unit of 2^n, wherein n is a positive integer including 0.

Kubota teaches the column address as being group by unit of a, b...m (see Fig. 2), wherein a<b<...<m. This is a similar system to the claimed invention as evidenced to reduce power consumption, this design incentive of avoiding peak current in the display memory device by addressing column in groups, would have prompted a predictable variation of Kubota.

Therefore, the claimed subject matter would have been obvious to one ordinary skill in the art a the time the invention was made.

Regarding **claims 15, 17, 19 and 21**, limitations within are similar to claim 4, 5, 6, and 7, same rejection applies.

Regarding **claims 16, 18, 20 and 22**, limitations within are similar to claim 4, 5, 6, and 7, same rejection applies.

Regarding **method claims 8, 11, 12, 13 and 14**, limitations within are similar to claims 1, 4, 5, 6 and 7 respectively, same rejection applies.

Regarding **method claims 9, 23, 25, 27 and 29**, limitations within are similar to claims 2, 15, 17, 19 and 21 respectively, same rejection applies.

Regarding **method claims 10, 24, 26, 28 and 30**, limitations within are similar to claims 3, 16, 18, 20 and 22 respectively, same rejection applies.+

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to YUK CHOW whose telephone number is (571)270-1544. The examiner can normally be reached on 8-6 M-TH E.T..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Quan-Zhen Wang can be reached on (571) 272-3114. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Y. C./
Examiner, Art Unit 2629

/Quan-Zhen Wang/
Supervisory Patent Examiner, Art Unit 2629